In the claims:

Cancel Group II, claims 13-19.
Cancel Group III, claims 22-35.

1. (original) A non-volatile memory array for continuous simultaneous writing and erasing of data comprising:

a plurality of parallel word lines and a plurality of bit and programming lines, the word, bit, and programming lines configured to selectively apply bias voltages;

a multiplicity of memory cells aligned in rows between the word lines and receptive of said bias voltages, each memory cell having a non-volatile memory transistor and an adjacent current injector, the word lines having parallel poly plates in capacitive relation therewith with a portion of each poly plate carrying word line induced voltage to a memory transistor and to a current injector in different rows; and

whereby memory cells associated with a first row can be written to with word line voltage while memory cells in a second row can be simultaneously erased with the same voltage.

2. (original) The apparatus of claim 1 wherein each non-volatile memory transistor is symmetrically paired with another non-volatile memory transistor.

3. (original) The apparatus of claim 1 wherein current from the current injector flows to the memory transistor causing charged particle creation from impact ionization, the charged particles stored in the gate of memory transistor.

4. (original) The apparatus of claim 3 wherein the current from the current injector is measured by an electrode having an applied bias.

5. (original) The apparatus of claim 1 wherein each injector has a fast diode and a control transistor interacting at a sufficiently proximate range so as to cause impact ionization of charged particles some of which are stored in the memory transistor.

6. (original) The apparatus of claim 1 wherein the non-volatile memory transistor and adjacent current injector are in side-by-side relation.

7. (original) The apparatus of claim 6 wherein the non-volatile memory transistor and the adjacent current injector are separated by an isolation region.

8. (original) The apparatus of claim 1 wherein each memory cell has at least two mutually connected floating gate transistors.

9. (original) The apparatus of claim 1 wherein different rows of the memory array have different doping densities, thereby establishing different threshold voltages in different rows.

10. (original) The apparatus of claim 9 wherein memory transistors of common thresholds are disposed in a row, with different rows having different thresholds.

11. (original) The apparatus of claim 10 wherein different rows of memory transistors span a range of thresholds.

12. (original) The apparatus of claim 1 wherein each memory cell is associated with an electrically communicating current meter measuring stored charge in the memory cell.

13-19. (Cancelled)

20. (original) A non-volatile memory array for continuous writing and reading of data comprising:

a plurality of parallel word lines and a plurality of perpendicular paired bit and program lines, the word, program, and bit lines configured to have selectively applied bias voltages;

a multiplicity of memory cells disposed in rows associated with the word lines, each memory cell having a transistor and an adjacent current injector, adjacent word lines having poly plates in capacitive relation with electrically communicating regions, extending from the poly plates into the transistor and the current injector, whereby memory cells in a first row can be programmed as memory cells in a second row are erased.

21. (currently amended) A method of simultaneously writing and erasing memory cells ~~handling data~~ in a non-volatile semiconductor memory array of the type having word lines and bit lines comprising:

selecting a first memory cell in the memory array using a word line and a bit line;

writing data to the selected memory cell ~~at least one specified address in a first row in a non-volatile memory array~~; and

simultaneously using said word line to select a second memory cell and erasing data whereby a single word line selects two memory cells for simultaneous write and erase operations ~~at an address other than the specified address in a row adjacent to the first row in said array~~.

22-35. (Cancelled)